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VLSI Implementation of High Speed 16 Bit Adder for Image Processing Application

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***Abstract*: This project is primarily deals the construction of 16 bit high speed on adder. The motivation behind the investigation is that an adder is a very basic building block of Arithmetic Logic Unit (ALU) and would be a limiting factor in performance of Central Processing Unit (CPU) . In this research article, we will present fast 16 bit adder with some approximation technique which is used in arithmetic application. For application analysis i am using edge detection where i am using my proposed Adder. Using this application i will prove that proposed adder having very less error which is tolerable by human eye. This project is design on Xilinx-14.1 and simulated on Modelsim. Application analysis will be done on Matlab for the application of Sobel edge detection. Image quality analysis will be done by PSNR, SSIM, FSIM and RFSIM.**

Keywords: **Central Processing Unit (CPU), Arithmetic Logic Unit (ALU), PSNR, SSIM, FSIM and RFSIM, VLSI.**

I. INTRODUCTION

There are two important challenges that the world of computing is facing. Currently, the first challenge is due to the increasingly ubiquitous nature of the present day portable electronics ranging from mobile phones to GPS-based navigation devices. Portability demands lower energy consumption without compromising on the functionality. Also, demand for low energy consuming, also referred to as green design, electronics [1] is gaining a lot of momentum.

According to the 2008 International Technology Roadmap for Semiconductors (ITRS) "Energy Consumption has become an increasingly important topic of public discussion in recent years because of global C02 emission .In general, the ITRS documents the impressive trends and, more importantly, sets aggressive targets for future electronics energy efficiency, for example, computational energy/operation (per logic and per memory-bit state changes). The most detailed targets relate directly to semiconductor materials, process and device technologies, which form the bases of integrated-circuit manufacturing and components, respectively." [2]

The core of every microprocessor, digital signal processor (DSP), and data processing application- specific integrated circuit (ASIC) is its data path. It is often the crucial circuit component if die area, power dissipation, and especially operation speed are of concern. At the core of data-path and addressing units in turn are arithmetic units, such as comparators, adders, and multipliers. Finally, the basic operation found in most arithmetic components is the binary addition. Besides of the simple addition of two numbers, adders are also used in more complex operations like multiplication and division. But also simpler operations like incrementing and magnitude comparison base on binary addition.

Therefore, binary addition is the most important arithmetic operation. It is also a very critical one if implemented in hardware because it involves an expensive carry-propagation step, the evaluation time of which is dependent on the operand word length. The efficient implementation of the addition operation in an integrated circuit is a key problem in VLSI design. Productivity in ASIC design is constantly improved by the use of cell based design techniques — such as standard cells, gate arrays, and field programmable gate arrays (FPGA) — and by low- and high-level hardware synthesis. This asks for adder architectures which result in efficient cell-based circuit realizations which can easily be synthesized. Furthermore, they should provide enough flexibility in order to accommodate custom timing and area constraints as well as to allow the implementation of customized adders.

The second challenge is manufacturing reliable and predictable electronic devices. Moore's Law predicts that the number of transistors on a single die is going to increase at an exponential rate. This has been accomplished by decreasing the size of an individual transistor up to 20nm where particular layers such as the gate oxide layer are about 1.2 nrn (equivalent to 5 atoms!). But engineering considerations on lithography have limitations of designing these tiny elements precisely which leads to hindrances like thermal noise, parametric variations and other device perturbations [3,4,5] which leads to unreliable computing. Again the 2008 ITRS report states as a long term challenge "Dealing with fluctuations and statistical process variations". Also the paper mentions that "Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control". [2]

These two challenges have competing requirements in the design of a VLSI system. A straightforward method of lowering the energy consumption is to lower the supply voltage of the circuit. But this would lead to transistors behaving unreliably because noise becomes a dominant factor. To ensure reliability, techniques such as redundancy and majority voting [6] can be used. However these techniques tremendously increase the energy consumption of the circuit. Thus conventional methods typically have contradictory results and do not offer a common solution to both energy consumption and reliable design.

The conventional electronic circuit design methodology utilizes three parameters in the tradeoff argument, the energy consumption of the circuit, the area occupied by the circuit and the speed at which the circuit is being operated. To face the challenges outlined previously, a radically new solution to introduce a new alternate dimension, the accuracy of the circuit, to the traditional design approach has been proposed recently. For the first time ever, Palem [7,8], showed that noise (or randomness) can be exploited as a resource for low energy but still obtain useful computation.

Currently there are three different techniques, applicable in different scenarios that use this novel fourth dimension in circuit design [9,10,11]. The first approach uses CMOS circuits that operate probabilistically due to noise [12]. The concept of a probabilistic CMOS switch (PCMOS) was introduced where a PCMOS inverter is correct with a probability parameter p ::: 1. The probabilistic inverter has been characterized in detail in terms of the relation between its energy consumption per switching and its probability of correctness. These probabilistic inverters were then used to design bigger probabilistic gates which switch correctly with a probability of correctness. This work was later extended to develop a probabilistic Boolean logic, because it was realized that conventional Boolean logic was no more valid in the universe where devices are probabilistic and not deterministic [13]. In probabilistic Boolean logic, the basic operators are defined with a probability of correctness, for example, an AND gate with a probability of correctness p is defined as /\p. Further extending the foundational probabilistic Boolean logic, a probabilistic arithmetic was developed, where the operators are also defined with a probability of correctness, such as + p.

II. OVERVIEW

Inexact circuit design is a design philosophy where the conventional constraint of requiring 100% accuracy in circuits is relaxed. Fundamentally, this philosophy adds a fourth dimension of accuracy to the current 3-dimensional circuit design space spanning around power consumption, area and delay. This methodology is applicable in the following two situations.

- The first situation is where the circuits are inherently "unreliable" and "probabilistic". Increasing parameter variations, noise susceptibility and decreasing process sizes are causing CMOS devices to be non-deterministic. To address these issues and precisely model the effect of these probabilistic circuit elements, the metric of accuracy needs to be introduced into the entire circuit design framework.

- The second situation is where the circuits themselves are not probabilistic in nature but are deterministic, but the application does not demand 100% accuracy. In such cases, relaxing the very rigid constraint of accuracy can be used to decrease energy consumption which is one of the leading challenges in current day circuit design.

The first challenge in adopting an inexact circuit design methodology is to prove that circuits with less than 100% accuracy can still be used to perform useful computations in many applications which are energy constrained. There are two types of applications where inexact circuit design can be implemented. They are

- The first set of applications is where randomness is a required quality. For example, many encryption applications use pseudo-random number generators to produce random numbers. But if there was a circuit that was inherently random then the extensive overhead of a pseudo-random number generator can be removed. That there are numerous such

applications/algorithms which actually benefit from having a circuit which is inherently probabilistic. Some of the algorithms are Bayesian inference, Random neural networks, probabilistic cellular automata, and hyper-encryption.

- The second set of applications where accuracy can be relaxed is where a less than 100% correctness can be tolerated. This set primarily consists of traditional digital signal processing (DSP) applications whose output is consumed and judged by a human being. For example, consider a music player whose quality can be tuned based on how much battery power is left. In fact, many DSP algorithms are "approximate" in nature. The discrete Fourier transform, for example, represents the entire signal in the frequency spectrum with a few samples, thus introducing both quantization and sampling error. However, this still works because the human brain can interpret stimuli to the body's senses and obtain useful information even if they are not completely accurate.

There are many researchers provide a many types of Approximate ADDERS and Multipliers.

In [13] the author proposed a new novel adder targeting to reduce the area and increase the speed of the circuit. The work is as shown in below first splitting the input operands into two parts: an accurate part that includes higher order bits and the inaccurate part that includes remaining lower order bits. Length of each part need not be equal and depends upon MAA′s and AP′s of application. The addition process starts from the joining point towards the two opposite directions simultaneously. Since the higher order bits play more important role than the lower order bits, normal addition method is applied for accurate part to preserve its correctness.

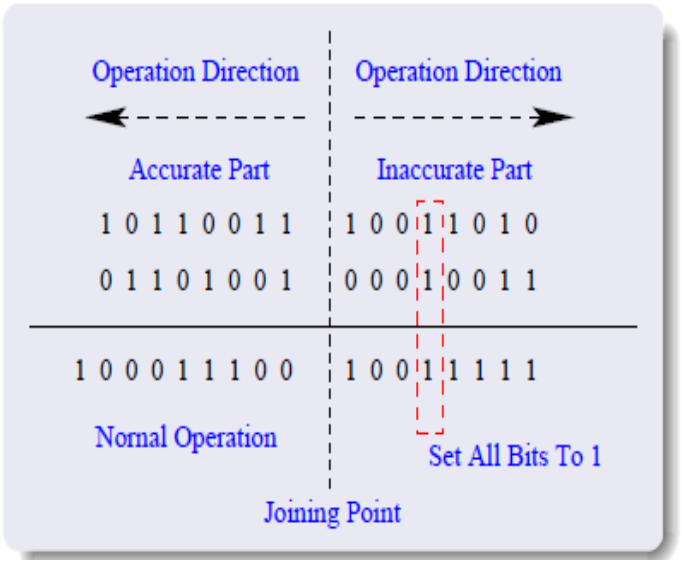


Figure 1. Error Tolerant Adder Type I (ETAI)

For inaccurate part no carry signal will be generated or taken in at any bit position to eliminate the carry propagation path. To minimize the overall error due to the elimination of the carry chain, a special strategy is adapted:

- Check every bit position from left to right,
- If both input bits are “0”or different, normal one-bit addition is performed and the operation proceeds to next bit position,
- If both input bits are “1”, the checking process stopped and from this bit onwards, all sum bits to the right are set to “1”.

By eliminating the carry propagation path in the inaccurate part and simultaneously performing addition in two separate parts, the overall delay and power is reduced. But the accuracy of the ETA-I is poor for small input numbers. In ETA-I the AP’s are strong function of input range and degrades as input range decrease, but AP′s are 100% for large input range.

III. ERROR-TOLERANT ADDER

To solve small number addition problem, ETA-II[14] was proposed by Zhu. ETA-II splits the entire carry propagation path into a number of short paths and completes the carry propagations in these short paths concurrently. The below figure shows the architecture and approach.

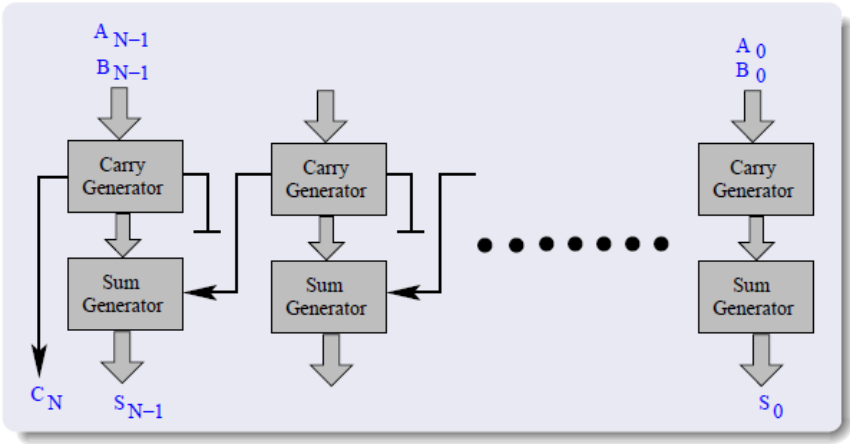


Figure 2. Block diagram of Type II ETA (ETAII)

In binary addition, worst-case happens when the carry signals are generated at the LSBs and propagates along the carry chain to the MSBs. If this worst case happens, tremendous amount of time and power will be consumed. As the worst case seldom happens, hence for most of the cases, this carry signal can be determined by just considering several input bits on the right of the current bit position. In ETA-II[14], an N − bit adder is divided into M blocks (M _ 2). Each block contains N/M bits and consists of two separate circuitries – Carry Generator and Sum Generator. The carry generator creates the carry-out signal and does not take carry-in signal from previous block and, hence the carry propagation only exists between two neighboring blocks. The longest carry propagation path of ETA-II is 2N/M and, hence worst-case delay of ETA-II is only 2/M times of the conventional adder. The accuracy of ETA-II for large input operands is degraded than ETA-I. The degraded accuracy for large input may still restrict ETA-II use.

In modified ETA-II [14] design, the higher order bits should be more accurate than the lower order bits. In modified structure, the first three carry generators are cascaded together to generate the carry signals. In this way, the carry signal for the highest block is generated by the preceding 12 bits and the carry signal for the others block is generated by the preceding 8 bits.

The approximate designs have difficulty of detecting and correcting errors, since they are designed for error-acceptable applications with target accuracy. In some applications, however, more accurate or totally accurate results are required under certain conditions, e.g., image processing in security cameras. In contexts where the required accuracy changes during runtime, the accuracy of results should be configurable to maximize the benefit of approximate operations. Figure illustrates how power benefits can be achieved with an accuracy-configurable design.

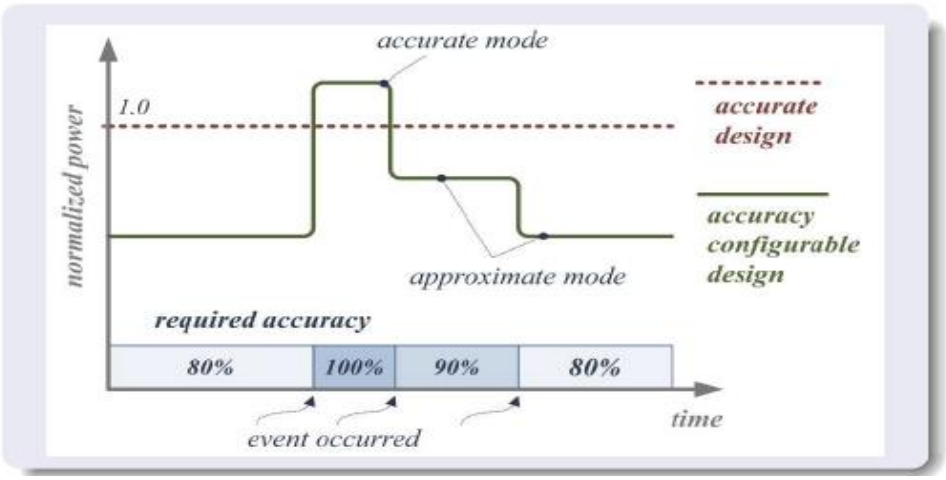


Figure 3 . Accuracy and power graph

The Accuracy Configurable Adder (ACA) [16] adder has feature of runtime accuracy configurability for better trade-off between accuracy, performance, and power. In ACA adder, the carry chain is cut to reduce critical-path delay, and sub-adders generate results of partial summations to increase accuracy.

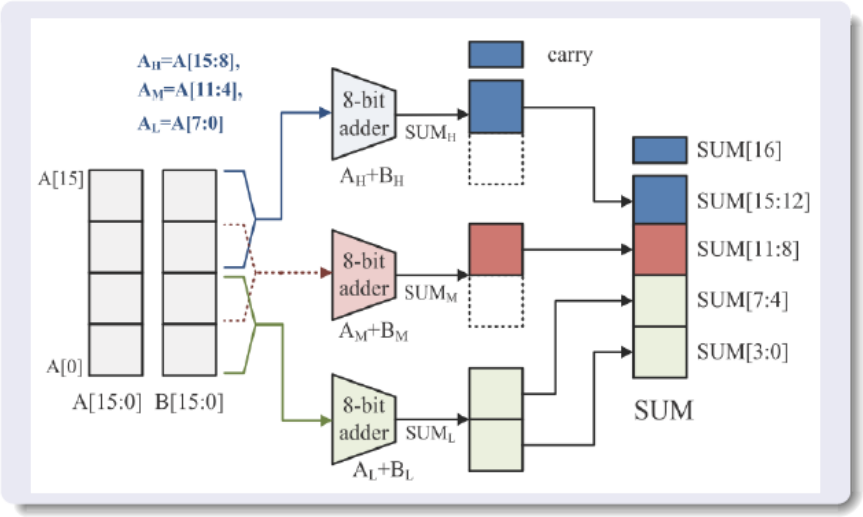
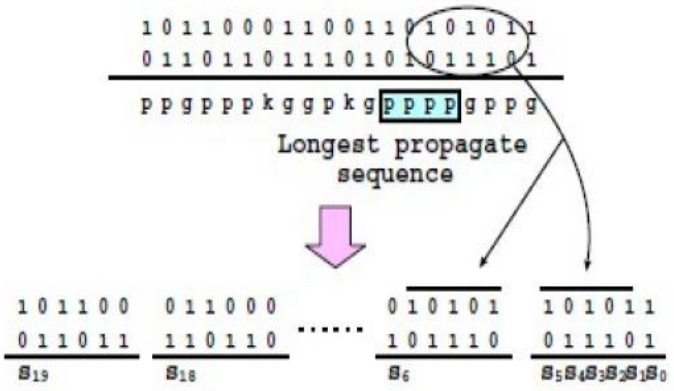


Figure 4 . ACA

Without the middle sub-adder, for random input patterns the error rate is 50.1%, whereas with the introduction of the middle sub-adder, error rate is reduced to only 5.5%.



In this paper [24] they took a specific case of 20 bit VLSA, which have two elements: 20 bit almost correct adder and an error detection circuit. In order to add two n-bit integers A and B, one can define generate, propagate and kill signals at each bit position as follows: The binary integers are denoted by uppercase letters, e.g., A, B are n bit binary numbers; the ith least significantbit of an integer A is denoted by ai. In order to add two n-bit integers A and B, one can define generate, propagate and kill signals at each bit position as follows:

gi = aibi

pi = ai xor bi

ki = ai + bi

IV. RESEARCH GAP

Many authors develop imprecise but simplified arithmetic units, which provide an extra layer of power savings over conventional low-power design techniques. This is attributed to the reduced logic complexity of the proposed approximate arithmetic units. Note that the approximate arithmetic units not only have reduced number of transistors, but care is taken to ensure that the internal node capacitances are much reduced.

Due to the limitations in these methods and the accuracy level requirements still the complexity can be reduced and the SPAA metrics can be still achieved efficiently. To improve SPAA metrics we need a novel arithmetic unit with low power, high speed, with increased density and PVC aware circuits.

As we can see in previous existing approaches are facing many problems which we are already discussed on research gap. So here we can resolve those issues. So the main focus is on performance and accuracy, but we do provide some numbers for the arithmetic units relating to energy and power. This is to provide an estimate of the amount of energy and power consumed by the units we choose to implement. The priorities of some new objective regarding this area are:

1) Robust and safe circuits.

2) Design time

3) Area/speed balance

The set of RMS [21] workloads is examined next in terms of usage, mathematical models, numerical algorithms, and underlying data structures. In image processing and many other DSP applications, the computational process of FFT involves a large number of additions and multiplications. Applications exclaim for approximate designs:

- Recognition, Mining, Synthesis (RMS) Applications,
- Human Sense Applications, and
- Inherent Error Applications.
- Image processing.

V. IMPLEMENTATION DETAILS

Here implementation of all existing approach is done by using Verilog HDl and design is done on Xilinx 14.2 and simulation is done on model sim. Here we show implemented output schematics in form of Lut and gate level:

Ripple carry: Thus, the adder is called ripple carry adder. The delay is a function of the number of stages. A ripple carry adder for an n-bit operand can be constructed by cascading n-full adders

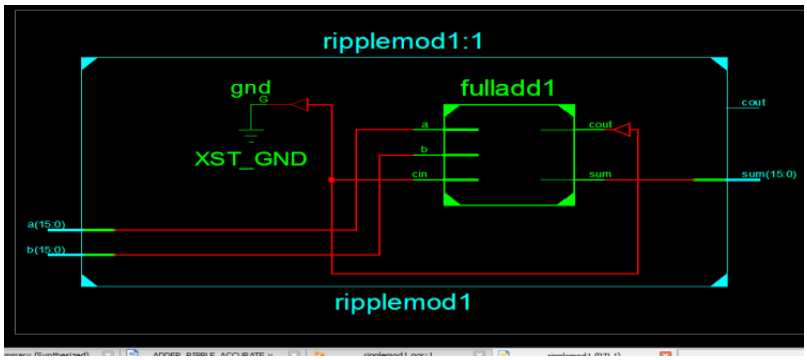


Figure 5. Ripple carry schemetic

Carry Save Adder:

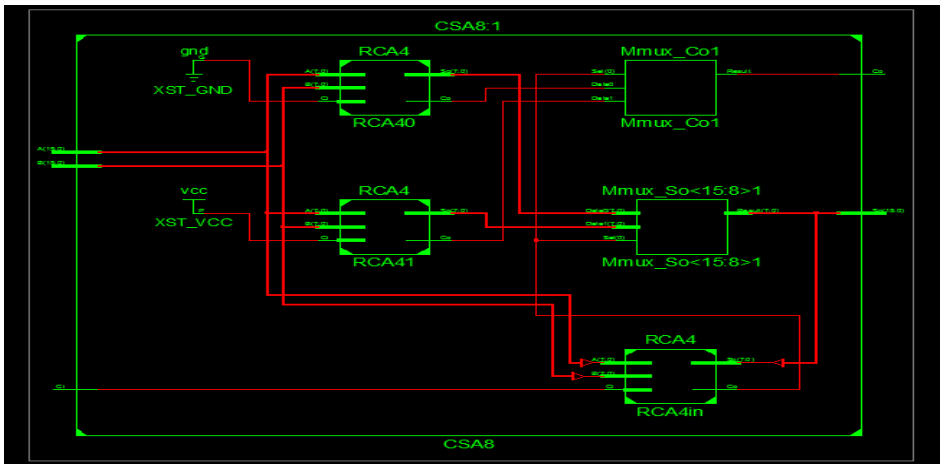


Figure 6 . Carry save schemetic

Carry look Ahead: Fast adders look-ahead to predict the carry out in an N-bit adder. The look-ahead adders remove the ripple carry effect by generating a carry for each bit simultaneously. The delay to add two N bit numbers no longer depends upon N, but on the logarithm of N, which is smaller. Here, all the required carry outputs are computed in parallel based on propagate and the generate signals.

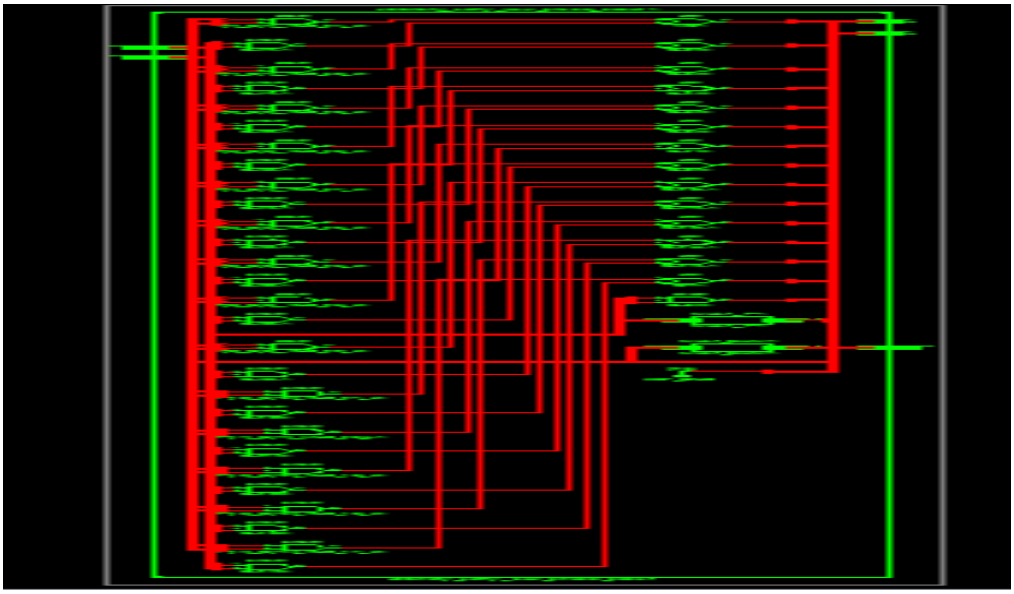


Figure 6 Carry look ahead schemetic

ACA: The Accuracy Configurable Adder (ACA) [16] adder has feature of runtime accuracy configurability for better trade-off between accuracy, performance, and power. In ACA adder, the carry chain is cut to reduce critical-path delay, and sub-adders generate results of partial summations to increase accuracy

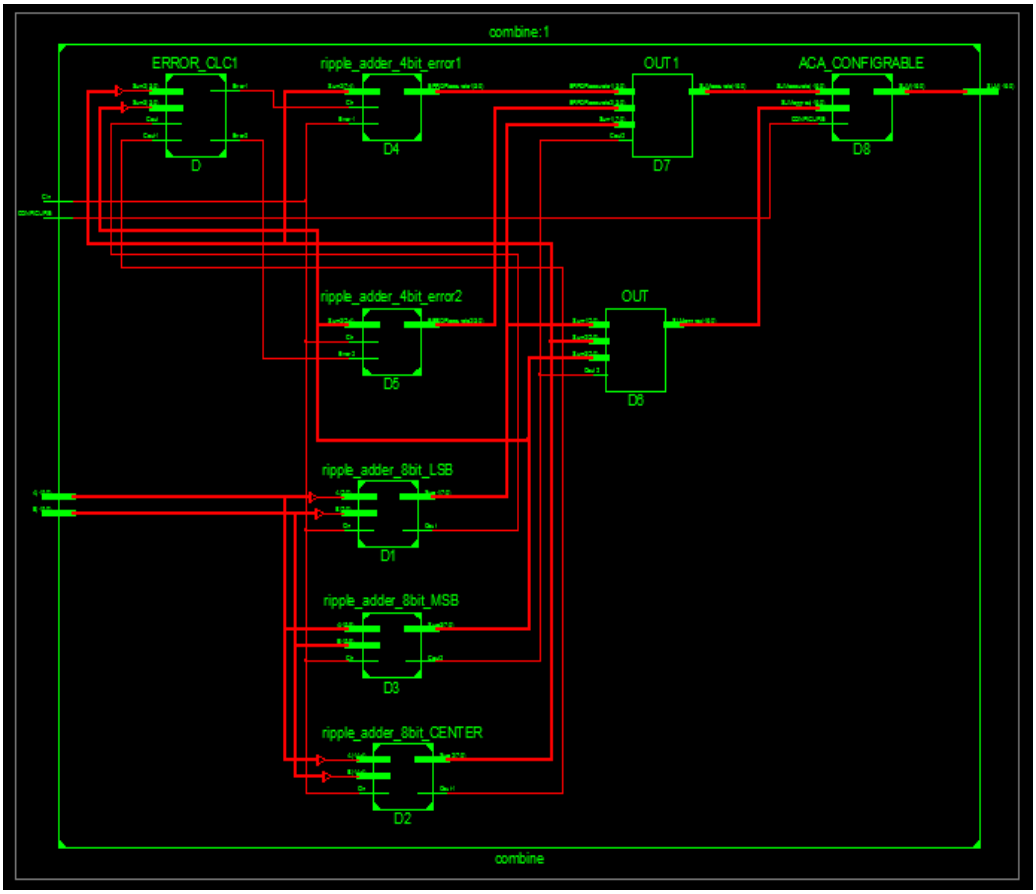


Figure7. ACA schemetic

ETA: There are many different types of adder such as ripple carry adder , look ahead adder , carry save adder . but all these have some problem regarding their speed and problem. A common solution to these speed and power is ETA by compromising a bit of accuracy. It can attain great improvement in both speed and power

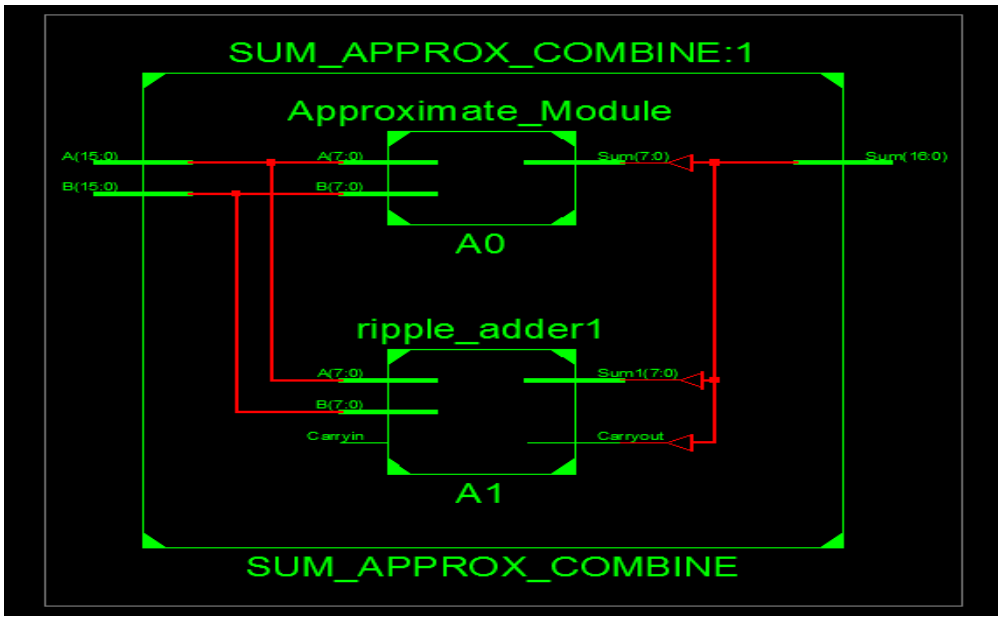


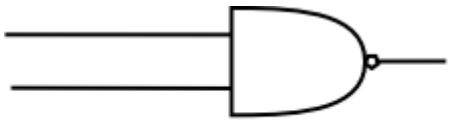
Figure 8. ETA schemetic

VI. PROPOSED METHODOLOGY

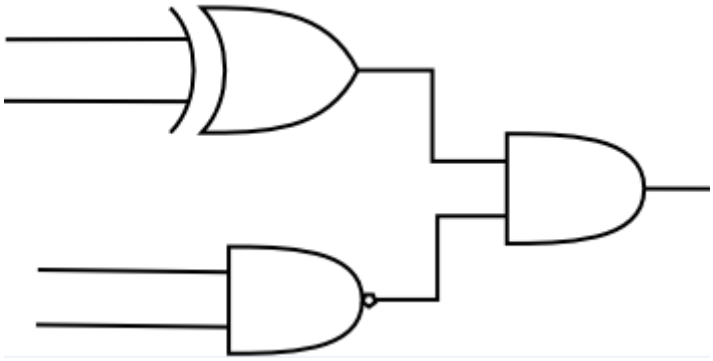
Proposed Architecture of 16 Bit approximate adder:

Here we proposed a new architecture of half adder and full adder as we know for 16 bit addition. Here we divide our 16 bit adder in three blocks first one is Approximate for lbs bit, second is semi accurate for higher lsb part. At last there is third block of accurate 8 bit adder for MSB part. In proposed approach we propose a new novel 16 bit architecture where we can put some error on lsb bit of adder. Here in approximate half and full adder there is no any carry generation unit. Here at approximate adder section we directly put 1 upto 4 bit after that for next four bit we will use our proposed approximate half and full adder than as last section we will use accurate half and full adder. So as we can see with small error generation we can reduce the hardware requirement and we can make justice with SPAA matrices.

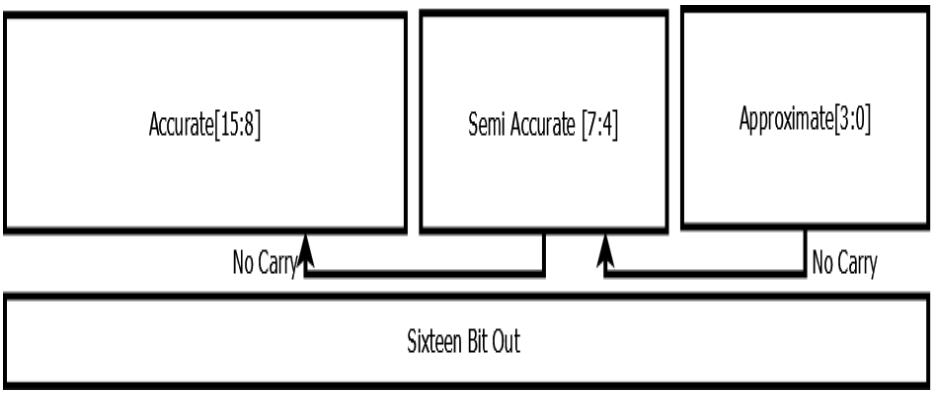
Proposed Approximate Half Adder:



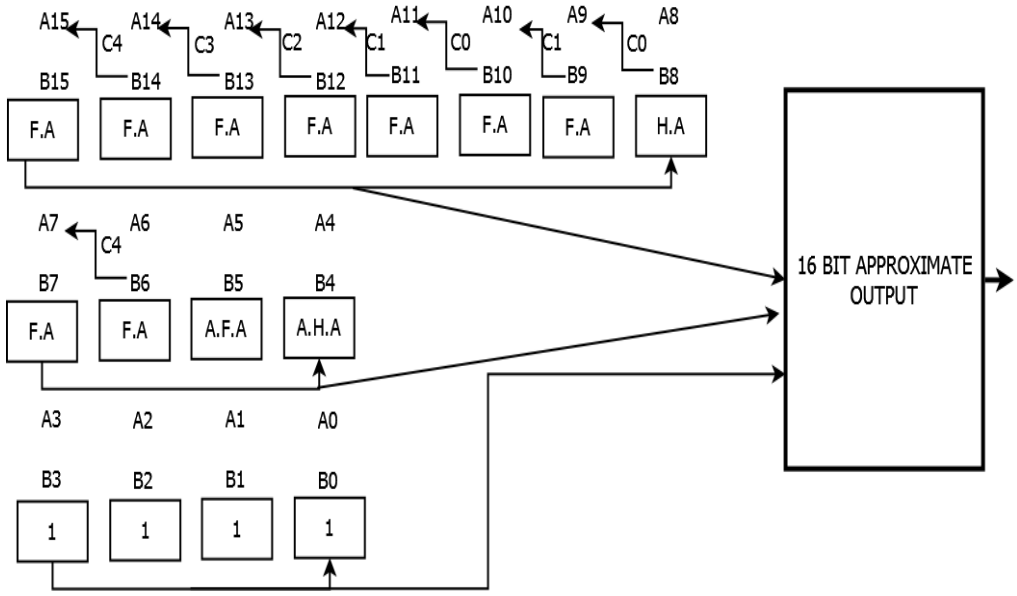
Proposed Approximate Full Adder:

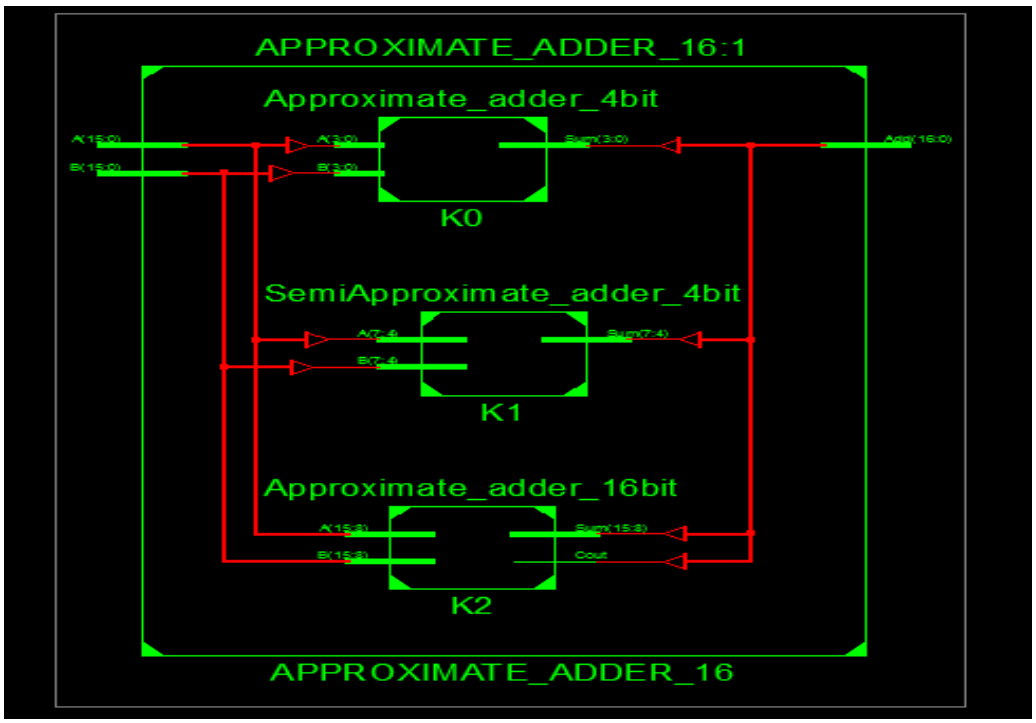


Proposed Generalize Architecture of 8 Bit Approximate Adder:

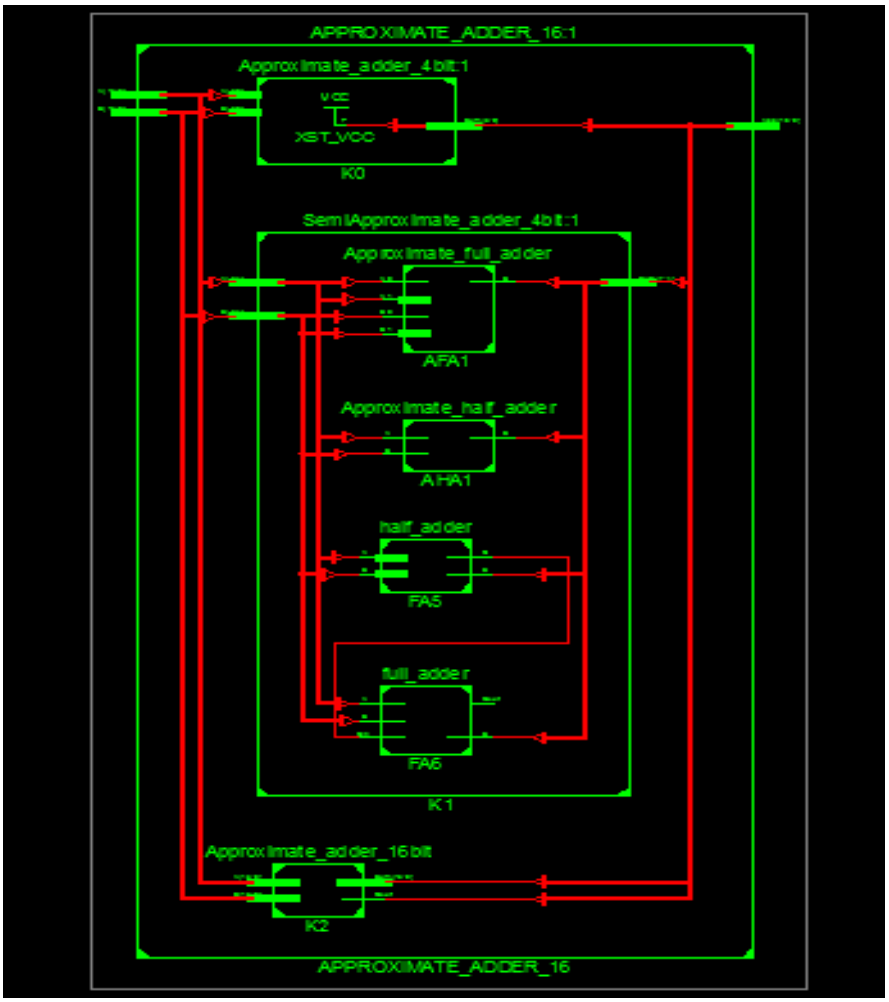


Proposed Architecture:





Proposed schematic:



Parameters to evaluate the Image:

Various parameters are used to evaluate the proposed algorithm at both levels. The various parameters are

1. PSNR (Peak signal-to-noise ratio)
2. SSIM (STRUCTURAL-SIMILARITY-BASED IMAGE QUALITY ASSESSMENT)[26]
3. Gradient Magnitude Similarity deviation (GMSD))[27]

1. PSNR:- The ratio between the maximum possible power of a signal and the power of disturbed noise that affects the accuracy of its representation. Because many signals have a very wide dynamic range. PSNR is usually expressed in terms of the logarithmic decibel scale. PSNR is most commonly used to measure the quality of reconstruction of lossy compression units (e.g., for image compression). The signal in this case is the original data.

2. SSIM (STRUCTURAL-SIMILARITY-BASED IMAGE QUALITY ASSESSMENT)[26]:-

Pixel based to structural based. Represents structure of objects in the scene, independent of the average luminance & contrast. Luminance is mean intensity of pixel its standard deviation is normalized contrast and structure is information. The structural similarity (SSIM) index value is between 0 to 1.

3. Gradient Magnitude Similarity Deviation (GMSD)[27]:

A good image quality assessment (IQA) model is expected to be not only effective (i.e., deliver high quality prediction accuracy) but also computationally efficient. Planning to the need to deliver image quality measurement tools in high-speed networks, the efficiency of an IQA metric is particularly important due to the increasing proliferation of high-volume visual data. Explanation a new effective and efficient IQA model, called gradient magnitude similarity deviation

VII. RESULT & ANALYSIS

In this section we represent image quality analysis in 16 bit sobel edge detection dn also here we represent hardware result in form of Lut, Delay and frequency. Here as we can see there is no any quality degradation on this application due to very small error in architecture.

Image quality Analysis:

Here for this analysis we are using some image quality parameters and those parameters are:

PSNR

SSIM [26]

GMDS [27]

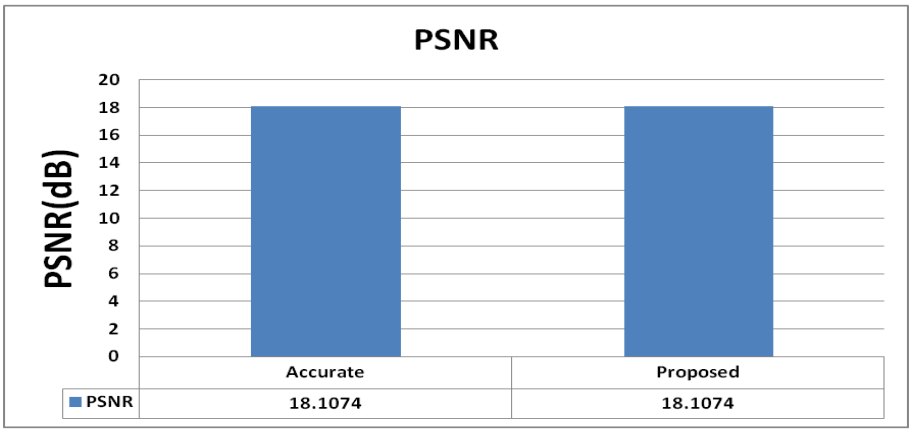


Figure 9 comparative result of PSNR

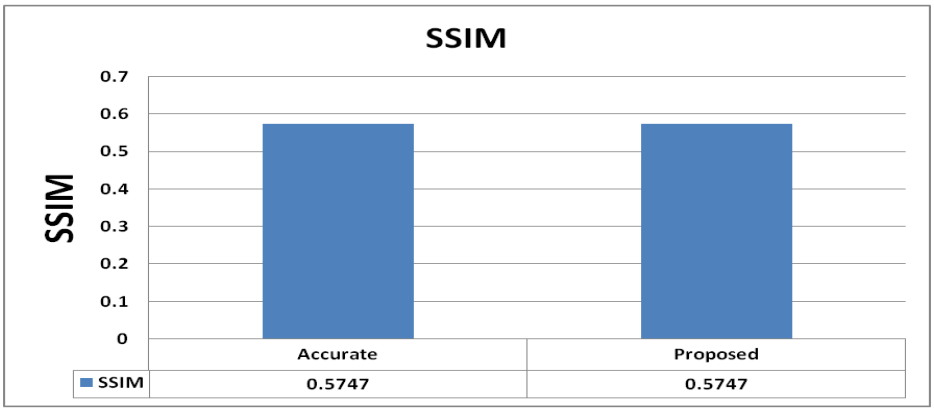


Figure 10 . Comparative result of SSIM

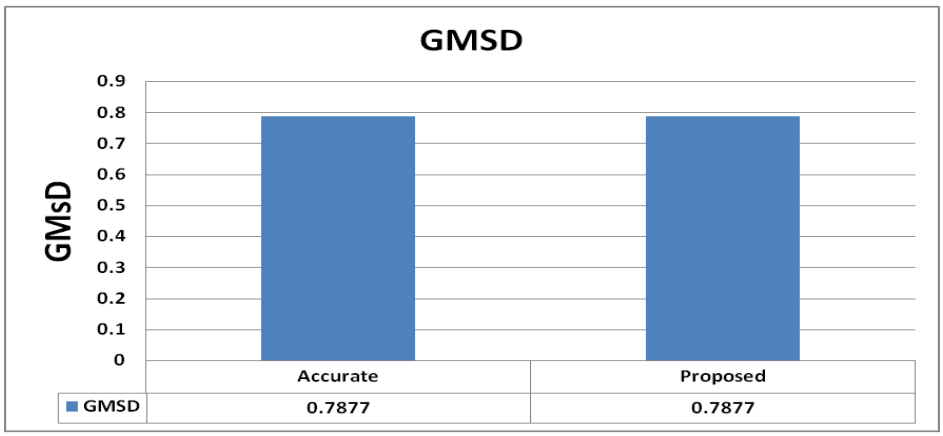


Figure 11 . Comparative result of GMSD

Hardware Analysis:

Here hardware analysis is done on 45nm based FPGA in term of:

- **LUT**
- **DELAY**
- **FRECQUENCY**

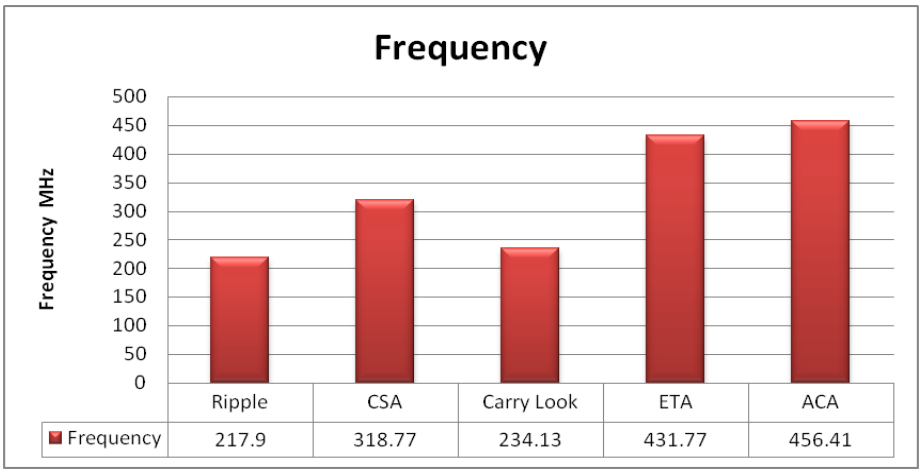


Figure 12 . Hardware analysis for frequency

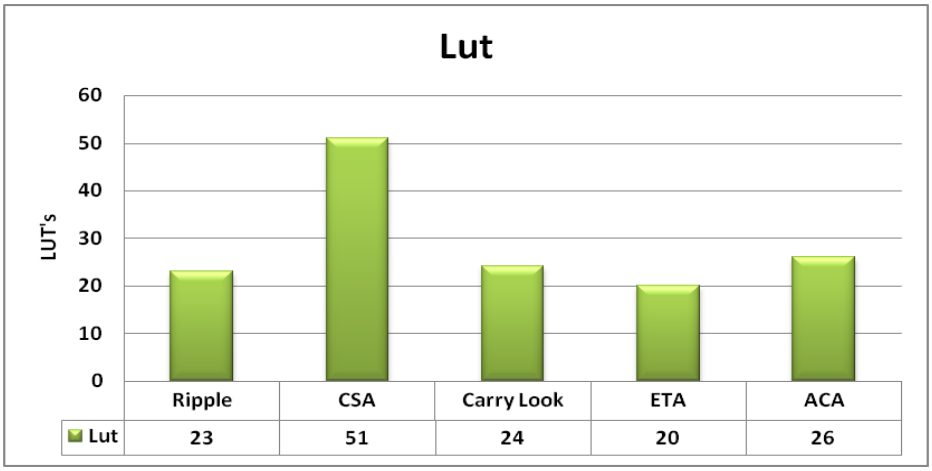


Figure 13. Hardware analysis for LUT

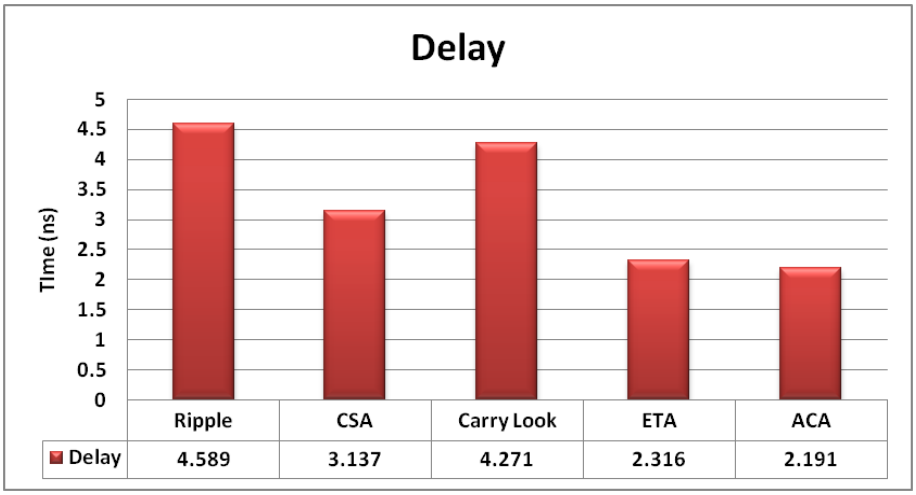


Figure 14. Hardware analysis for Delay

There is approximately 20-30% improvement is done of architecture as compare to previous existing approaches like ETA,ACA,CSA,CLA.RIPPLE.

VIII. CONCLUSION

In this thesis work we have proposed a 16 bit approximate adder, which is developed in verilog. Here as for the architecture point of view we have proposed a novel architecture which is combination of 3 blocks, First block is approximate adder, second block is semi accurate adder and third block is accurate adder. Here we are also proposing a basic architecture of adder which is known as full and half adder. Here for application point of view we are using 16 bit sobel edge detection where we got no any image quality degradation. Here at hardware level simulation result shows there is 20-30% improvement in previous exsisting architecture.

REFERENCES

[1] THE CLIMATE GROUP, "Smart2020: Enabling the low carbon economy in the information age," 2008.

[2] ITRS, "International technology roadmap for semiconductors update," 2008.

[3] K. Natori and N. Sano, "Scaling limit of digital circuits due to thermal noise," Journal of Applied Physics, vol. 83, pp. 5019-5024, 1998.

[4] N. Sano, "Increasing importance of electronic thermal noise in sub-0.1mm SiMOSFETs," The IEleE Transactions on Electronics, vol. E83-C, pp. 1203-1211, 2000.

[5] L. B. Kish, "End of Moore's law: Thermal (noise) death of integration in micro and nano electronics," Physics Letters A, vol. 305, pp. 144-149, 2002.

[6] J. von Neumann, "Probabilistic logics and synthesis of reliable organisms from unreliable components," in Automata Studies, 1956.

[7] K. V. Palem, "Proof as experiment: Probabilistic algorithms from a thermodynamic perspective," in Proceedings of the International Symposium on Verification (Theory and Practice)" June 2003.

[8] K. Palem, "Energy aware computing through probabilistic switching: a study of limits," Computers, IEEE Transactions on, vol. 54, pp. 1123 - 1137, sep. 2005.

[9] J. George, B. Marr, B. E. S. Akgul, and K. Palem, "Probabilistic arithmetic and energy efficient embedded signal processing," in Proceedings of the The IEEEIACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, pp.158-168,2006.

[10] 10. L. N. Chakrapani, K. K. Muntimadugu, A. Lingamneni, J. George, and K. V. Palem, "Highly energy and performance efficient embedded computing through approximately correct arithmetic: a mathematical foundation and preliminary experimental validation," in CASES '08: Proceedings of the 2008 international conference on Compilers, architectures and synthesisforembedded systems, (New York, NY, USA), pp. 187-196, ACM,2008.

[11] A. Lingamneni, C. Enz, J.-L. Nagel, K. Palem, and C. Piguet, "Energy Parsimonious Circuit Design through Probabilistic Pruning," Proceedings of the Design Automation and Test in Europe, 2011.

[12] P. Korkmaz, B. E. S. Akgul, L. N. Chakrapani, and K. V. Palem, "Advocating noise as an agent for ultra low-energy computing: Probabilistic CMOS devices and their characteristics," Japanese Journal of Applied Physics, vol. 45, pp. 3307-3316, Apr.2006.

[13] Zhu, Ning, et al. "Design of low-power high-speed truncation-error-tolerant adder and its application in digital signal processing." Very Large Scale Integration (VLSI) Systems, IEEE Transactions on 18.8 (2010): 1225-1229.

[14] Zhu, Ning, Wang Ling Goh, and Kiat Seng Yeo. "An enhanced low-power high-speed adder for error-tolerant application." Integrated Circuits, ISIC'09. Proceedings of the 2009 12th International Symposium on. IEEE, 2009.

[15] Zhu, Ning, Wang Ling Goh, and Kiat Seng Yeo. "Ultra low-power high-speed flexible Probabilistic Adder for Error-Tolerant Applications." SoC Design Conference (ISOCC), 2011 International. IEEE, 2011.

[16] Kahng, Andrew B., and Seokhyeong Kang. "Accuracy-configurable adder for approximate arithmetic designs." Proceedings of the 49th Annual Design Automation Conference. ACM, 2012.

[17] Gupta, Vaibhav, et al. "IMPACT: imprecise adders for low-power approximate computing." Proceedings of the 17th IEEE/ACM international symposium on Low-power electronics and design. IEEE Press, 2011.

[18] Lu, Shih-Lien. "Speeding up processing with approximation circuits." Computer37.3 (2004): 67-73.

[19] Venkatesan, Rangharajan, et al. "MACACO: Modeling and analysis of circuits for approximate computing." Proceedings of the International Conference on Computer-Aided Design. IEEE Press, 2011.

[20] Liang, Jinghang, Jie Han, and Fabrizio Lombardi. "New metrics for the reliability of approximate and probabilistic adders." Computers, IEEE Transactions on62.9 (2013): 1760-1771.

[21] Chen, Yen-Kuang, et al. "Convergence of recognition, mining, and synthesis workloads and its implications." Proceedings of the IEEE 96.5 (2008): 790-807.

[22] Venkataramani, Swagath, et al. "SALSA: systematic logic synthesis of approximate circuits." Proceedings of the 49th Annual Design Automation Conference. ACM, 2012.

[23] Shin, Doochul, and Sandeep K. Gupta. "A re-design technique for datapath modules in error tolerant applications." Asian Test Symposium, 2008. ATS'08. 17th. IEEE, 2008.

[24] Verma, Ajay K., Philip Brisk, and Paolo Ienne. "Variable latency speculative addition: A new paradigm for arithmetic circuit design." Proceedings of the conference on Design, automation and test in Europe. ACM, 2008.